HIGH VOLTAGE THIN FILM TRANSISTORS INTEGRATED WITH MEMS

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ABSTRACT

The integration of high-voltage thin film transistors with a released MEMS process onto the same substrate is demonstrated. High voltage transistors capable of 800 V actuation voltage are used to actuate released metal cantilevers and membranes with a low temperature fabrication process (< 350 ˚C) on glass substrates. This demonstration is an important step towards realizing MEMS arrays with integrated addressable drivers for applications which require high voltage, such as electrostatic MEMS devices on low temperature substrates (e.g. glass or flex). High voltage thin film transistors (HVTFT) provide the unique property of easily controlling high voltage (50 V to 800 V) using a standard input voltage range (0 V to 20 V). To our knowledge this is the first demonstration of integrated HVTFT actuating released MEMS structures.

Keywords: thin film transistor (TFT), high voltage, electrostatic actuation, integrated drivers

INTRODUCTION

While the majority of commercial MEMS are based on high temperature silicon fabrication processes, there is a growing interest in low temperature processes and materials. Processes with low peak processing temperature (< 350 ˚C) are more compatible with glass substrates, flexible plastic substrates and post-CMOS on silicon processes. Glass substrates are particularly important because the flat panel display industry already produces thin film transistor (TFT) circuits on large glass substrates for significantly less cost per area then silicon circuits. Currently glass substrate areas are 4 m^2 while silicon substrates are only 0.1 m^2.

There are numerous applications for MEMS on low temperature substrates. Devices that directly interface with human length scales require large chips and are most economically fabricated on large area glass substrates. Digital dis-

plays and imagers are probably the largest chips (100s to 1000s cm^2) [1], but printed paper documents for reading also suggests printer head designs with large chips (10s of cm^2). Paper movers based on airjets require large printed circuit board substrates [2]. Similar examples include tactile displays for the blind and finger print sensors. Glass substrates are also often required for their optical transparency (for optical MEMS) or high frequency loss properties (for RF and microwave MEMS). Flexible substrates are important for displays, large area pressure arrays for robotic sensing, and more recently electronic textiles.

Electrostatic MEMS actuators are candidates for many of these applications. For example, moving cantilevers and membranes can be used to form valves, ejectors, scanners, mirrors and variable capacitors. Electronics integration can improve performance and the size of the system, but high voltage is often required for the drivers, particularly if appreciable force is required. Traditional silicon circuits can provide the high voltage drivers for integrated MEMS, but not directly on low temperature substrates [3, 4]. High voltage thin film transistors (HVTFT), however, can be fabricated with standard TFT technologies on both glass and flex substrates. HVTFT are based on standard amorphous silicon (α-Si) technology with the major difference being an offset near the drain contact. This offset region enables high breakdown voltage on the drain electrode while voltages for the gate and source electrodes can be kept low (Figure 1). PARC has previously demonstrated twelve inch wide arrays of thousands of HVTFT on 64 μm pitch for electrographic plotting applications [5]. The HVTFT can be integrated with low voltage TFT circuits. PARC has already built amorphous silicon TFT based shift registers with 400 KHz clock rates, as well as polysilicon TFT ring oscillators operating at 4.9 MHz (< 0.01 μsec propagation delay per inverter stage) [6].

This paper describes a low temperature fabrication process which integrates HVTFT with released MEMS structures on glass substrates. Electrostatic actuation of metal beams is demonstrated with integrated HVTFT drivers. HVTFT inverter circuits are used to actuate curved beam cantilevers. While there has been some limited previous work on integrating thin film transistors with field emitter tips and other devices [7-10], to our knowledge this is the first demonstration of HVTFT integrated with and actuating released MEMS structures.

FABRICATION

The fabrication process is performed on glass wafers (Corning 1737) with the HVTFT built first followed by the MEMS process. The HVTFT uses standard sputtering and plasma enhanced chemical vapor deposition (PECVD) deposition techniques. The completed HVTFT (Figure 2a) consists of multiple layers patterned with photoresist lithography and wet etching. They include the gate layer (80 nm molybdenum-chrome), gate dielectric (300 nm silicon nitride), active semiconductor (50 nm amorphous silicon), gate dielectric (300 nm silicon nitride), contact layer (100 nm heavily doped n-type amorphous silicon), and source and drain metal (50 nm titianium-tungsten, 100 nm aluminum, 50 nm chrome). The drain of the HVTFT is also used as the bottom electrode for the electrostatic MEMS capacitor.

To fabricate the MEMS structures, PECVD was used to deposit a passivation layer (300 nm silicon nitride) followed by a sacrificial release layer (2 μm silicon). After patterning contact vias (Figure 2b), an adhesion layer (100 nm titanium) and electroplating seed layer are sputtered (150 nm gold). To make the structural layer (Figure 2c), the gold was patterned with the MEMS layer mask and then the structural layer was electroplated (1.7 μm copper). During the electroplating, the titanium was used as a plating mask, but photoresist could also be used. To release the cantilevers and membrane structures, the titanium was cleared, and than an isotropic xenon diflouride etch was used to clear the silicon sacrificial layer, producing the final structure (Figure 2d).

The peak temperature for the entire process is 350˚C. This is low enough for glass substrates as well as many flexible substrates, such as polyimide. Lower peak temperatures (< 275˚C) are also possible, enabling the use of plastic substrates. The entire process could be performed on top of a silicon wafer with pre-fabricated low voltage CMOS logic circuits, which electrically control the HVTFT and MEMS.

INTEGRATED ACTUATION

An image of a completed device is given in Figure 3. A HVTFT with gate length of 9 μm, width of 10 μm and offset of 6 μm, is connected to a cantilever bridge which is 360 μm long by 50 μm wide and 1.7 μm thick. Mechanical actuation controlled by the on-chip HVTFT is depicted in Figure 4. With a 70 V power supply on an external bias resistor and the gate at 0 V, the HVTFT is off and the beam sees 50 V and deflects down ~0.5 microns. As the gate is turned on to 20 V the drain voltage is reduced and the beam rises back to a straight position. The deflection was measured with a laser interferometer (Zygo New View 200).

INVERTER ACTUATION

For array applications it is preferable not to have an off-chip bias resistor for each driver. An inverter circuit using HVTFT which does not require off-chip resistors is demonstrated in Figure 5. With 0 V to 5 V input range, the output can be varied between 95 V and 20 V. This inverter was used to actuate a curved out-of-plane cantilever made from stress-engineered metal (Figure 6)[11]. The curved cantilever uses a unique tapered side electrode configuration which overcomes the snap-down problem associated with electrostatic actuation [12]. Approximately 70 μm of displacement normal to the substrate is controlled with 0 V to 5 V. This particular cantilever was on a separate chip from the inverter but the curved beam cantilever process is a low temperature metal MEMS process which is compatible with the HVTFT process.

FUTURE WORK

We have fabricated HVTFT with a > 300 V breakdown, as demonstrated in Figure 7. This transistor has a width of 50 μm, length of 9 μm, and an offset of 6 μm. Recently we have also demonstrated operation at 800 V by increasing the offset to 100 μm (Figure 8). As the gate voltage is swept from -5 V to 15 V the drain current increases four orders of magnitude. The HVTFT have also been integrated with released membranes (Figure 9a) and are ready for future testing. Other MEMS devices which are candidates for HVTFT integration include 3D scanning metal mirrors that have been fabricated in a compatible low-temperature process (Figure 9b). Possible applications for such mirrors include smart optical switch matrices or adaptive optics on low temperature glass or flex substrates

CONCLUSIONS

High voltage thin film transistors have been successfully integrated with a low temperature (< 350˚C) metal MEMS process on glass substrates. Integrated actuation has been demonstrated. This is a critical step towards realizing large arrays of integrated drivers and MEMS on low cost and large area substrates such as glass and flex.

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FIGURES

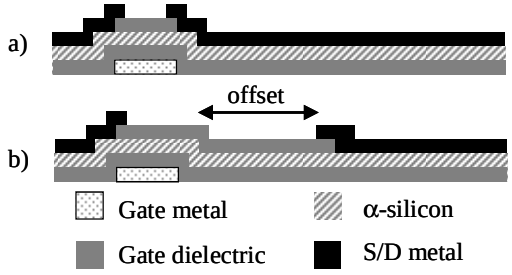


Figure 1. Device structure of (a) standard α-Si TFTs and (b) High voltage α-Si TFTs. Note the added offset region, which breaks the source/drain symmetry of standard TFTs but enables high operating voltages.

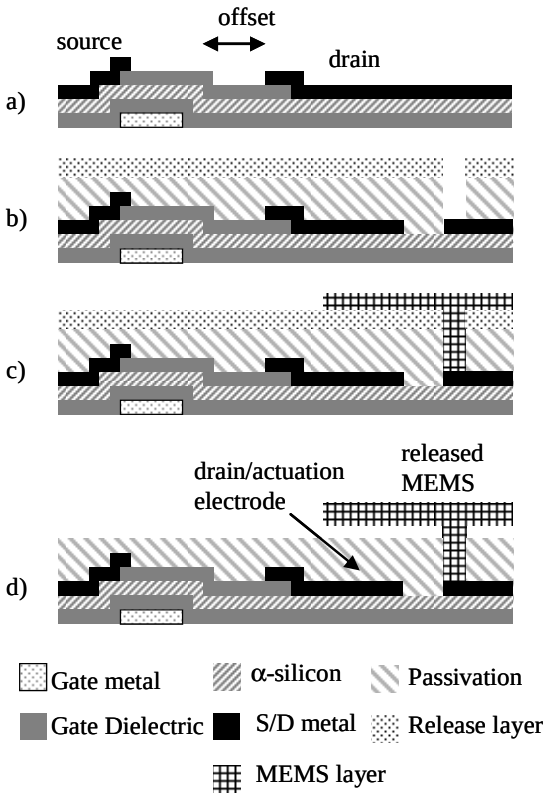


Figure 2. Process flow schematic for integrating high voltage thin film transistors (HVTFT) with released metal MEMS. a) Build a bottom gate amorphous silicon thin film transistor. b) Deposit and pattern the interlayer dielectric and sacrificial layer. c) Deposit and pattern the MEMS metal layer. d) Etch away the sacrificial layer to release the MEMS. The HVTFT drain metal serves as the bottom electrode for the MEMS.

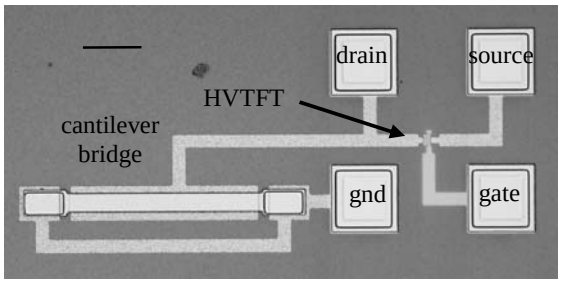


Figure 3. Photograph of a fabricated high voltage thin-film transistor integrated with a released double-clamped beam.

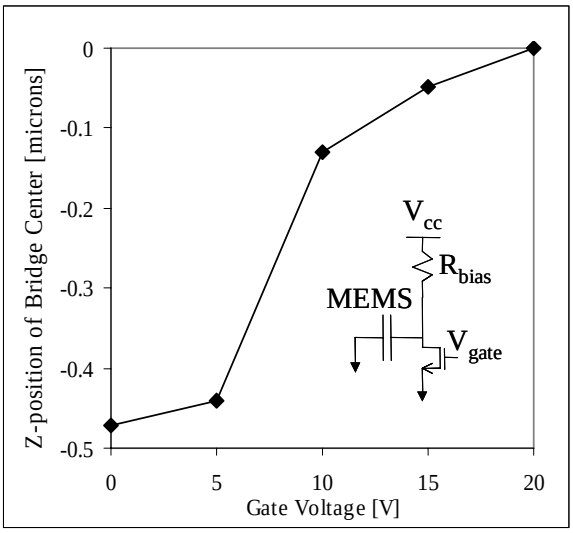


Figure 4**.** Measured vertical position of the center of the cantilever bridge in Figure 3 as a function of the applied gate voltage on the HVTFT.

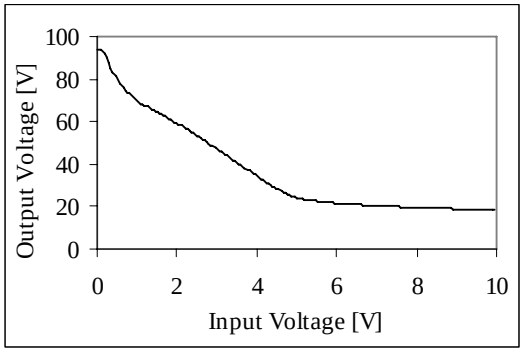


Figure 5. Measured output curve of a HVTFT inverter.

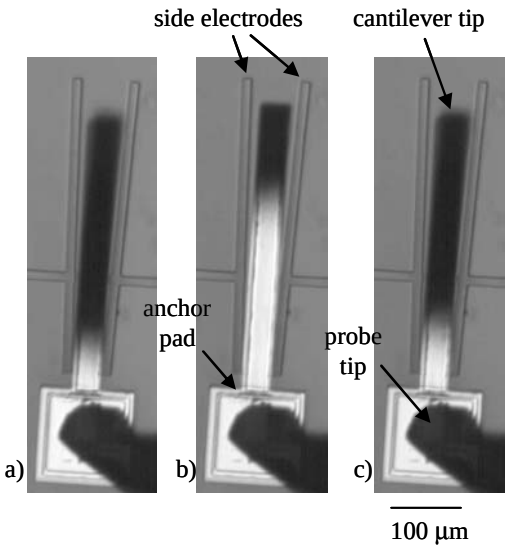


Figure 6. Optical images of a moving out-of-plane bent cantilever (on a separate chip) being actuated by the inverter. The cantilever rolls down and up smoothly when controlled by the inverter input voltage. The vertical position of the cantilever tip moves ~70 μm, from a height of ~90 μm (a), to a height of ~20 μm (b), and then back to ~90 μm (c). The cantilever is 30 μm wide, 350 μm long, 1.5 μm thick, and curls up 90 μm above the surface when not actuated.

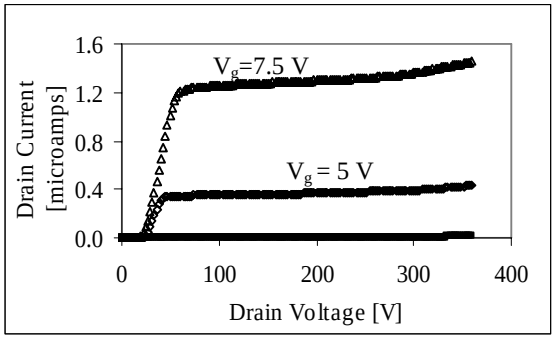


Figure 7. HVTFT IV curve showing breakdown voltages in excess of 300 V. Drain current versus drain voltage is shown for different gate voltages.

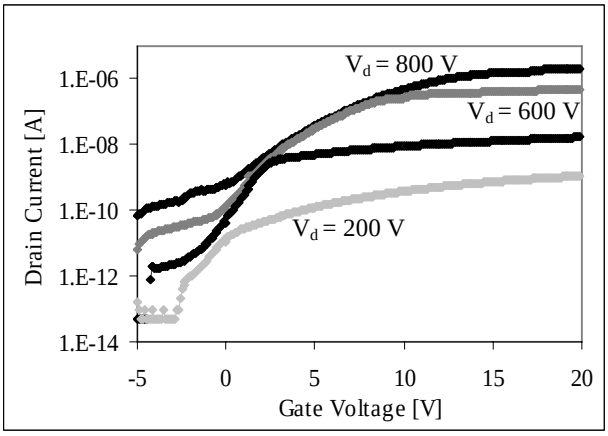


Figure 8. Measured drain current as a function of gate voltage as the drain voltage is swept from 200 V to 800 W. The dimensions of the dimensions of the HVTFT are W = 15 μm, L = 10 μm, offset = 100 μm.

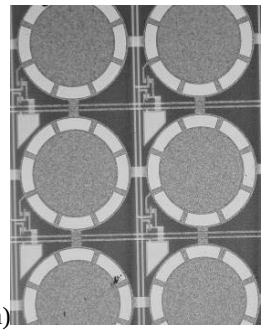
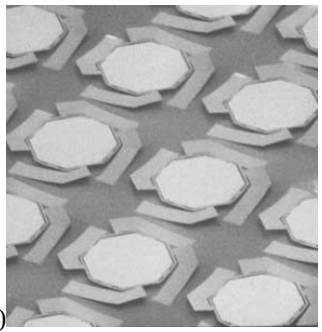
a)  b) 

Figure 9. a) Example of a fabricated array of released MEMS diaphragms (500 μm diameter) with integrated high-voltage drive electronics. b) An array of scanning micro-mirrors on glass substrates. The mirror fabrication process is compatible for integration with the HVTFT drivers.

LIST OF FIGURES

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