Wafer Level Packaging with Soldered Stress Engineered Micro-Springs

Eugene M. Chow¹, David K. Fork¹, Christopher L. Chua¹, Koenraad Van Schuylenbergh² and Thomas Hantschel²

¹Palo Alto Research Center (PARC), 3333 Coyote Hill Road, Palo Alto, CA 94304 USA (email: echow@parc.com)
²IMEC, Leuven B-3001 Belgium
³Department of Physics, University of Antwerp, Wilrijk B-2610 Belgium

Index Terms: Compliant interconnects, wafer level packaging, probing, fine pitch, surface mount technology, flip chip, memory packaging, stress-engineered, cantilever, micro spring

Abstract

Micro springs for integrated circuit test and packaging are demonstrated as soldered flip chip interconnects in a direct die to printed circuit board package. The spring interconnects are fabricated with thin film metallization as the last step in a wafer-scale process. The z-compliance of the interconnects can be used to test and/or burn-in parts in wafer form. After the parts are diced from the wafer, the springs then become the first-level (and often the last-level) interconnect between the chip and the board. The xy-compliance of the interconnect enables considerably large die to be soldered to an organic printed circuit board without underfill using an SMT compatible process. To demonstrate this concept, daisy chain test vehicles were fabricated on die measuring 11.5 mm by 6.5 mm with 48 spring contacts on a 0.8 mm by 0.65 mm grid array, each spring measuring 400 µm by 100 µm. The parts were placed onto organic boards with screen printed solder paste using a pick and place machine. The parts were reflowed to complete the solder connection to each spring using eutectic and lead-free solder. Assembled parts have undergone >20,000 hot plate thermal cycles and >1000 oven thermal cycles without failure.

I. Introduction

In earlier reports, stress-engineered micro-springs have been demonstrated in dense arrays of 6 µm pitch interconnects [1], optoelectronic modules [2], 20 µm pitch pressure contact flip chips [3], and in high quality factor RF coils on BiCMOS circuits [4]. This paper addresses wafer level packaging (WLP), a term that refers to forms of packaging that require no added packaging materials once parts are diced from the wafer. WLP is a growing trend in
the integrated circuit (IC) industry. The term wafer level packaging implies a package-less package. The adoption of WLP has been driven by the trend toward increasingly smaller parts and the drive to lower costs, particularly in the portable electronics markets. Wafer level packaging is typically applied to integrated circuits on die with dimensions smaller than about 3 mm on a side, and with fewer than 36 contacts. These parts can be soldered directly to a printed circuit board using solder bump interconnects. The handling of these components is much like other surface mount technology (SMT) components. Once the parts are diced from a wafer, they can be placed onto a printed circuit board which has screened solder paste, and reflowed into place along with other surface mount components.

Wafer level packaging of larger die and with a high density of contacts is very challenging. For the same circuit board substrate, larger die imply a larger thermo-mechanical run-out during the solder reflow operation and also during operational cycles. For common combinations of materials, such as silicon ICs and FR4 printed circuit boards, the mechanical strain near the edges of a 1 cm chip can be tens of microns. The widely accepted lead-free alternative to eutectic solder, Sn-Ag-Cu, has a higher reflow temperature, exacerbating the strain induced during cool-down.

Compliant interconnects are an alternative to plastically deforming solder bumps. The ideal process for a compliant interconnect would have only batch fabrication steps (as opposed to serial processes like wire bonding), few masks, no expensive materials, conventional processing tools, and thus low costs. All of the approaches to compliant wafer level packaging approach these desired features in different ways with different tradeoffs. Among the solutions proposed for this application are metallization formed over organic elastomers [5,6], springs formed from wirebonds [7], and springs formed by electroplating through multiple layers of photoresist [8].

II. Interconnect Fabrication

Our approach to compliant wafer level packaging is to use controlled levels of stress to create curved cantilever springs that release and bend away from their substrate [9]. We create a stress gradient in a deposited layer of metal trending from compressive on the bottom, to tensile on the top. In its most common embodiment, two-lithographic masks are used to define the shape of the cantilever, where the cantilever lifts off of the substrate, and where the cantilever remains anchored. An image of the bent cantilever is shown in Figure 1 and a summary of the fabrication process given in Figure 2. The process steps to fabricate a stress-engineered micro-spring interconnect are as follows:
(1) deposit a sacrificial layer
(2) deposit a spring metal with a stress gradient
(3) pattern the spring metal
(4) mask the spring metal anchor
(5) release the springs with a selective etch
(6) over-plate metal onto the springs
(7) protect the springs for dicing
(8) dice completed parts from the wafer

We deposit a metallic sacrificial layer onto the substrate. This allows the springs to make electrical contact through vias. Strong adhesion is important because the sacrificial layer that is not removed needs to firmly hold the anchor portion of the cantilever in place on the substrate. Without sufficient adhesion, the cantilever might peel off. It is also important that the sacrificial layer be metallic so that electrical contact can be made through vias to underlying circuitry.

Stress in thin films is normally considered undesirable, as stress is often the culprit for cracking and delamination, which are clearly unwanted outcomes. With proper attention to process parameters, stress can be controlled and kept within limits that allow functional structures with high yield and uniformity. Uniform stress is critical in order to keep the spring lift-height uniform because the two key parameters for lift-height are the cantilever length and its bending radius. The bending radius becomes the critical parameter for process control, because it depends on the film thickness and the stress gradient, both of which depend on the process control. The bending radius, $R$ of a bent cantilever for a continuous, linear stress gradient, $\Delta \sigma$, a biaxial modulus of elasticity $Y'$, and a cantilever of thickness, $t$, is given by the formula

$$R = \frac{Y't}{\Delta \sigma}.$$  

Thin film stress is ordinarily measured by wafer curvature measurements before and after the film is deposited. We perform these measurements routinely as process monitors, however, two limitations of this measurement are that (1) it produces one stress value, which is a global average of the stress across the wafer, and (2) it is insensitive to directional anisotropies in the stress. One of the best monitors of the uniformity and isotropy of the stress...
across a wafer is the lift height, \( h \), of the springs because it depends on the radius, and length, \( l \), according to the function

\[
h = R(1 - \cos(l/R)).
\]

Figure 3 shows a series of 200 lift-height measurements on 160 \( \mu \)m long StressedMetal springs that were deposited and released on a 100 mm wafer. The springs span a distance of 90 mm across the wafer, and are arranged in clusters pointing in eight different directions. The heights were measured using a Nikon NEXIV VMR series computer numerical control video measuring system [10]. The data show a small systematic variation in lift height with direction (creating the width of the band of data) which we believe may be a pattern recognition effect. Without allowing for this effect, the max-min variation is about +/- 7% of the average lift height. This shows that the stress gradient across the wafer is both highly uniform and independent of direction.

The springs are released by masking the anchor portion of the spring with photoresist which protects the edges of the anchor and prevent undercutting. The cantilever portion of the spring is exposed to the etchant, which can rapidly undercut the spring metal to dissolve away the sacrificial metal. The process is carried out using a wet chemical etch which can be applied as a batch process taking between 1 to 2 minutes.

As Figure 2 illustrates, the springs are plated after their release. The over-plating serves several purposes, as plating adds thickness to the spring to provide additional stiffness and lowers the electrical resistance of the spring and its anchor by adding a parallel conduction path. Less resilient, but more conductive metals, such as copper can be added close to the center, neutral portion, of the spring, and more resilient metals can be plated toward the outer surfaces, since these portions are strained the most during spring flexure. An outer coating of noble metal such as gold can be plated onto the spring to provide resistance to oxidation.

The steps that we have described for the fabrication of springs are compatible with highly automated batch processes running on a wafer manufacturing line or wafer bumping line. Two masking steps are typically required to carry out the process. As plating becomes more mainstream in the IC fab, we see this technology as an enabler for replacing the last level of metal with a compliant interconnection that can be used for both test and packaging.

**III. Wafer Level Test and Packaging**

A key benefit of the spring interconnect technology is the ability to serve two purposes, first as a test contact and subsequently as a package interconnect. Figure 4 illustrates the concept of using microfabricated springs on the wafer for making the temporary connections needed to test and burn-in the components before dicing. In this
Illustration, the probe card is a flat contactor. One of the advantages of this approach is that the flat contacting device can be easily cleaned, for example with a polyvinyl alcohol brush. The flat contactor is also less expensive than a conventional probe card because much of the cost comes from the compliant interconnect. Once testing is completed, the packaging step can utilize the springs as part of the final assembly. Figure 5 illustrates the use of the springs as part of the package for direct connection between the chip and the board.

Ordinarily, the springs in a probe card are required to undergo $10^5$ to $10^6$ touchdowns. This places a stringent requirement on the reliability and contact force of the springs. As was illustrated earlier, the process for making the springs on a wafer is relatively simple, and only requires two masks. In the approach illustrated in Figure 4, new springs arrive with each new wafer, so the number of touchdowns is only on the order of several per spring. This relaxes the design requirements on the spring considerably since currently most wafers have aluminum pads which require significant amounts of force (~10 gf per spring) to scrub through the aluminum oxide surface. Our work on gold-on-gold electrical contacts suggests that stable electrical contact can be achieved with contact forces well under 1 gf. For example, in earlier work on pressure contacts we showed that a stable contact resistance can be achieved with a contact force of less than 5 mgf [11]. In other work we reported >10,000 fretting cycles without electrical glitches with a contact force of only 27 mgf [12]. In flip chip packages of 800 springs per package we observed no glitches or gradual resistance increases with ~10 mgf gold to gold contacts [3]. With a flat contactor, the reliability problem is turned around, and it becomes necessary to design pads that can survive many touchdowns. For this reason it may be necessary to replace the gold contact pad on the contactor with a more refractory noble metal such as rhodium.

**IV. Prototype System, DDR Memory**

We chose dynamic random access memory (DRAM) for prototyping because these components are manufactured in large volumes and require test and burn-in prior to end-use. The 11.5 mm by 6.5 mm test vehicle was modeled after a 48/60 FBGA chip scale package (CSP) for double data rate (DRR) DRAM. Its 48 springs were laid out in a radial fashion on a 0.80 mm x 0.65 mm grid according to the 48/60 FBGA footprint and wired up in pairs to form two-spring daisy chains (Figure 6). The mating FR4 board connected spring pairs together to form a single continuous daisy chain (Figure 7). Every daisy chain trace on the FR4 board was also routed to a connector to provide access to each spring pair during testing. Each board accepted two spring die.

The daisy chain arrays of micro-machined springs were fabricated on glass and on silicon wafers. The glass
used was Corning 1737 because it has a thermal expansion coefficient similar to that of silicon; yet, unlike silicon, it is transparent. This is convenient because it allows optical inspection of the solder reflow process around the springs during package assembly. It also allows visual monitoring of the springs before and after thermal cycling, humidity aging, and mechanical shock testing. The silicon-like thermal expansion coefficient ensures that the springs on glass would see similar thermal cycling stresses as those on a silicon chip would experience if packaged directly on FR4 boards.

The springs were fabricated using the process outlined in the previous section. The core spring material consists of a sputter-deposited molybdenum-chromium (MoCr) alloy with a built-in stress gradient. The appropriate stress profile for achieving a desired spring lift was obtained by controllably varying the ambient Argon pressure during sputter deposition. Gold was sputter-deposited beneath and on top of the stress-engineered MoCr layer to function as seed layers for electroplating. After the springs were formed and released from the substrate they were coated with additional layers of metal to improve their conductivity and to allow solder wetting during package assembly. The plated overcoats were typically 3.2 µm of Cu, followed by 1.3 µm of Ni and 150 nm of Au on each side of the springs.

The mating pads for the springs were made on standard double-sided FR4 boards (Park-Nelco N4000-11, a high Tg FR-4 designed for lead-free solders). We used 500 µm diameter landing pads oriented in a daisy chain pattern so they align with the springs during package assembly. The 71 µm thick copper pads (2 oz/ft²) were finished with approximately 150 nm immersion gold over 2.5 to 3 µm nickel, a standard finish for surface-mount solder reflow processing. The copper on the board backside underneath the spring die was left unpatterned. We tapped each segment of the daisy chain with electrical connections and routed those lines to the edge of the board so they could be connected to an external ribbon cable for easy monitoring during thermal cycling.

Just before package assembly, the boards were coated with Kester 951 liquid no-clean flux. The chemical was allowed to dry in air, and a solder paste was subsequently applied on the pads by stencil printing using a 25 µm (1 mil) chemically etched stainless steel stencil. We experimented with a variety of solder pastes, including Kester’s R244 Sn63Pb37 eutectic solder and Kester’s R905 Sn96.5Ag3.0Cu0.5 lead-free solder. We achieved excellent wetting with either solder.

Packages were assembled using a flip-chip look-up/look-down aligner tool where the spring, die and the
FR4 boards were held face to face against each other, aligned, and then brought together. The gap between the board and the spring die was set by 100 µm-thick spacers placed on the board at locations corresponding to the periphery of the spring die away from the springs. We applied beads of Loctite Hysol® 3515 Cornerbond adhesive on four locations of the board corresponding to the corners of the spring die prior to package assembly. The adhesive held the package together between assembly and solder reflow. The assembled packages were then moved to a sealed reflow oven where the appropriate temperature profile was applied in a nitrogen-rich atmosphere. This solder reflow step also cured the Cornerbond adhesive and transformed it into a hard solid mass. Figure 8 and Figure 9 depict the package cross section. Depending on the amount of over-plating and solder on the springs, the DC room temperature resistance of the 48-spring and trace daisy chain measured between 2 and 5 Ω.

V. Environmental Testing

The reliability tests reported here include thermocycle, humidity, mechanical vibration and mechanical shock testing. Table 1 summarizes the results which are discussed in detail below.

Initially, thermocycle tests were performed on a thermal cycle hot-plate incorporating a thermoelectric cooler and resistance cartridge heaters. A thermal conductive grease was placed onto the backside of the printed circuit board to ensure good thermal contact. A thermocouple was embedded into the space below the board. The hot plate was cycled between minus 10 °C and 150 °C with a cycle time of about 12 minutes per cycle. The daisy chain DC resistance was measured during the thermal cycle test at a current bias of 1 mA. A sample with lead-free solder and no corner bonds has presently lasted on the thermal cycle tester for a total of 20,600 thermal cycles. Because this sample lacks corner bonds, the springs must absorb the full thermal runout between the chip and the board. The DC resistance data for cycles 12532 through 13432 appear in Figure 10. The DC resistance is modulated by the temperature of the package due to the temperature coefficient of resistance of the metals in the package. Figure 11 shows data for several thermal cycles collected by the DC resistance measuring unit, showing the temperature and resistance tracking closely as expected.

Whereas the hotplate data showed the long term compliance of the springs, the cycle may be too fast to fully express solder creep effects. We therefore have added a liquid nitrogen cooled thermal cycle oven (Sigma Systems model M18) to our testing capability. This unit allows a more extensive temperature range, from -40 °C to 125 °C. The dwell time at each temperature limit is 15 minutes. The unit can cool at 56 °C/min, and it can heat at
18 °C/min. The oven thermal cycle profile is shown in Figure 12. While in the thermal cycle oven, the parts are tested using an AnalysisTech STD series event detector high speed glitch tester. This unit can detect momentary increases in resistance (above 100 Ω) that last longer than 200 ns, which are considered failures. Three out of three lead-free samples went through 0 °C to 100 °C for 1600 cycles followed by -40 °C to 125 °C for 1300 cycles without failures. These samples, like the previous ones, did not have corner bonds. For our cornerbonded packages, four out of four lead-free samples have survived 1037 cycles from -40 °C to 125 °C.

The humidity test condition is a soak at 85 °C at a relative humidity of 85% for 1000 hours or longer. The DC daisy chain resistance was measured before and after this soak. The sample used for humidity testing was a corner bonded glass chip. There was no change in the DC chain resistance after this measurement. To explore whether the assembly was weakened as a result of the humidity test, the sample was placed on the thermal cycle hot plate described earlier, and the DC chain resistance was measured during cycling from -10 °C to 150 °C for five measurement cycles. Neither the dwell at high humidity, nor the subsequent thermal cycling revealed any contact degradation.

To measure vibration reliability, parts were subjected to the JEDEC JESD22-B103-B standard mechanical vibration test. Boards were rigidly mounted onto a shaker and a laser vibrometer was used to measure acceleration and displacement. Simple harmonic motion with a continuously changing frequency from 5 Hz to 45 Hz was applied so that boards moved 0.75 mm of peak-peak displacement. From 45 Hz to 500 Hz three g’s of acceleration were applied. The sweeps lasted for 16 minutes and were repeated for each axis (48min total). The resistance of the chains on the packages did not change after the test. To confirm post-test continuity, packages were also subjected to 5 thermal cycles on the hotplate with in-situ resistance measurements. The results were identical to Figure 11.

Shock resistance was tested by bolting the board assembly (Figure 9) to an aluminum plate to prevent direct impact of the chip and to simulate the presence of an enclosure in a portable device. Parts were dropped 30 times from 0.5 m on an office floor to mimic a standard mechanical shock test (JEDEC Mechanical Shock Standard, JESD22-B104-B). Packages were dropped five times in each of the 6 possible orientations. Packages with corner bonds were found to have the same resistance before and after shock testing (2 of 2). Impact deceleration was measured with an accelerometer to be at least 400 g’s. The parts were also found to pass drop tests from heights of 1, 2 and 11 m, the latter height being limited by the height of the building where the tests were conducted.
VI. Summary and Conclusions

Thin film deposited, stress-engineered microsprings are a promising wafer level packaging solution for providing the vertical compliance needed for test purposes, along with the lateral compliance needed for large die to pass reliability testing. Once the parts are diced from the wafer, they can be assembled onto standard printed circuit boards using an SMT process. Results presented in this paper illustrate that the parts can survive thousands of thermal cycles as well as humidity and shock testing.

Acknowledgements

We thank Sven Kosgalwies, Lai Wong, Vicki Geluz-Aguilar, Eric Peeters, Jackson Ho, and Yu Wang for useful discussions and their help in fabricating the devices described herein. This work was supported in part by the NIST Advanced Technology Program under Award 70NANB8H4008
Figure 1. SEM micrograph of an array of StressedMetal springs. The springs are 400 µm long and 100 µm wide
Figure 2. Schematic steps used to produce StressedMetal springs. (A) A sacrificial layer is deposited onto the wafer, followed by a patterned island of stress-gradient metal with a built-in stress gradient. (B) A mask is applied to define where the cantilever will re-release, and the sacrificial layer is etched. (C) Additional metal is plated onto the released spring.
Figure 3. Spring lift-height measurements across a 90 mm section of a 100 mm wafer
Figure 4. A wafer with springs being used for test contact with a flat contactor
Figure 5. An illustration of wafer level fabricated-springs being used for connection to a printed circuit board.
Figure 6. Section of the StressedMetal mask showing two die, the springs laid out in a radial fashion to match a 48/60 FBGA footprint, and various alignment marks to guide chip-to-board placement.
Figure 7. Test board layout with daisy chain traces brought out to edge connectors to facilitate electrical access during testing.
Figure 8. Illustration of an assembled package
Figure 9. Picture of an assembled package
Figure 10. DC daisy chain resistance during thermal cycling.
Figure 11. Temperature and resistance data from several thermal cycles.
Figure 12. Oven thermal cycle temperature profile.
Table 1. Summary of environmental test results.

<table>
<thead>
<tr>
<th>Solder</th>
<th>Assembly</th>
<th>Test</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>R905 lead free</td>
<td>no adhesive</td>
<td>thermocycle hotplate</td>
<td>-10 °C to 125 °C for 20,600 cycles</td>
<td>2 of 2 pass</td>
</tr>
<tr>
<td>R905 lead free</td>
<td>no adhesive</td>
<td>thermocycle oven</td>
<td>0 °C to 100 °C for 1,600 cycles followed by -40 °C to 125 °C for 1,300 cycles</td>
<td>3 of 3 pass</td>
</tr>
<tr>
<td>R905 lead free</td>
<td>Cornerbond</td>
<td>thermocycle oven</td>
<td>-40 °C to 125 °C for 1037 cycles</td>
<td>4 of 4 pass</td>
</tr>
<tr>
<td>R244 lead-tin</td>
<td>Cornerbond</td>
<td>humidity oven</td>
<td>85 °C, 85% RH for 1,000 hrs</td>
<td>7 of 7 pass</td>
</tr>
<tr>
<td>R244 lead-tin</td>
<td>Cornerbond</td>
<td>mechanical vibration</td>
<td>sine sweeps 5 Hz to 500 Hz, 0.75 mm amplitude, 3 g acceleration, 3 axis</td>
<td>2 of 2 pass</td>
</tr>
<tr>
<td>R244 lead-tin</td>
<td>Cornerbond</td>
<td>mechanical shock</td>
<td>drop 0.5 m each axis orientation, 30 times total</td>
<td>2 of 2 pass</td>
</tr>
</tbody>
</table>
References


