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Persistent photoconductivity effects in printed n-channel organic transistors

Tse Nga Ng, Ichiro Fujieda, Robert A. Street, and Janos Veres
Palo Alto Research Center, 3333 Coyote Hill Road, California 94304, USA
Department of Electrical and Electronic Engineering, Ritsumeikan University, Kusatsu 525-8577, Japan

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Persistent photoconductivity of top-gate n-type organic transistors is investigated. The irradiation of green light leads to a negative shift in transistor threshold voltage and an increase in sub-threshold current. These light-induced effects are enhanced when the gate is negatively biased during the light irradiation, and the recovery process is faster at 60°C than at 25°C. After storage in dark, full recovery is obtained for a transistor printed with a neat semiconductor, whereas for the device printed with a solution of the same semiconductor mixed with an insulator, only partial recovery is observed after four days at room temperature. Other stress conditions (irradiation with a positive gate bias, irradiation without bias, and bias under dark) do not change the threshold voltage or the sub-threshold current significantly. We attribute this photo phenomenon to holes trapped and released at the dielectric/semiconductor interface and a smaller number of positive fixed charges generated in the bulk of the semiconductor layer. © 2013 American Institute of Physics.

I. INTRODUCTION

Among the numerous types of thin-film transistors (TFT),1 organic thin-film transistors (OTFTs)2 are particularly suited for low-cost applications because they can be fabricated on a flexible substrate by high throughput, low-temperature processes such as printing. Recent theoretical analysis on the potential of new organic semiconductors3 and a demonstration of high-mobility OTFTs4 are promising for the development of printed electronic applications. For many applications such as large-area displays and photosensors,5,6 an intense light source is often near the transistors. Although a light-shield is usually placed on a transistor, such a shield is often not perfect and stray light may lead to persistent photoconductivity (PPC), a phenomenon where conductivity of a material remains high for a while after light irradiation.

Understanding the PPC effects in OTFTs is crucial for practical applications, and the light response provides a method to identify problems in fabrication processes and/or device materials that affect stability of a transistor. Hoffman et al. reported that ultraviolet radiation causes PPC in ZnO-based oxide transistors due to surface oxygen adsorption.7 Ghaffarzadeh et al. studied PPC in passivated Hf-In-Zn-O TFTs and identified ionization of oxygen vacancy sites caused by visible light.8 Nomura et al. observed threshold voltage shift in In-Ga-Zn-O transistors under negative-bias-light stress, and they attributed its origin to the holes trapped at the semiconductor-insulator interface.9 For optical sensor applications, PPC limits maximum rate of operation for repetitive usage. A three-terminal gate structure is reported to suppress the persistent photocurrent in an oxide semiconductor photo-transistor.10 While many researchers have investigated photo-instability in oxide semiconductor devices11 and the PPC effects in p-type OTFTs,12–16 the number of reports on n-type OTFTs17 is limited. Understanding this effect on both p- and n-type semiconductors are important for development of stable complementary circuits.18–20 In this paper, we report our experiment on PPC in top-gate, n-type OTFTs fabricated by all-additive inkjet printing processes. We discuss the changes observed in the transfer characteristics and explain the origin of PPC in these transistors.

II. FABRICATION PROCEDURE

The printed OTFTs are top-gate structures on a plastic polyethylene naphthalate substrate. The silver electrodes (300 nm thick) and the semiconductors (100 nm thick) are deposited by inkjet process.21 The transistor dielectric is a spin-coated teflon, with capacitance $C_t = 4.5 \text{ nF/cm}^2$. Two types of semiconductors are inkjet printed: one is a neat solution of a polyethylene derivative provided by Polyera22 and the other is the same material blended with an insulating polymer poly-$\pi$-methyl styrene in 3:1 ratio.23 The net amount of semiconductor is the same for both types of ink, as both solutions have 15 mg/ml of semiconductor, without or with 5 mg/ml poly-$\pi$-methyl styrene added. The insulating polymer is used to mitigate coffee ring formation in the printed features. The p-type semiconductor blend is known to go through vertical phase separation dependent on the substrate surface energy24 and enhanced electrical stability against bias stress.25 We have not yet been able to determine whether phase separation occurs in the n-type blend here, but future analysis using techniques such as secondary ion mass spectroscopy may reveal the film composition in more details.

III. RESULTS

We irradiated n-type OTFTs with the setup shown in Fig. 1(a). A light emitting diode (LED) emitting green light is used as the light source with power of 1.2 milliwatt per cm$^2$ measured at the sample stage. As shown in Fig. 1(b), the light from the LED is scattered by the stage and a fixed...
amount of scattered light reaches the transistor. A cross-section of this OTFT is schematically illustrated in Fig. 1(c).

All the electrical characterizations described in this paper were carried out in air at the temperature of 25°C unless noted otherwise. The PPC phenomenon is observed as the OTFT transfer characteristics is shown to shift with irradiation and then slowly recover during storage in the dark. The shift increased when the irradiation took place during the measurement, in which the gate bias $V_g$ was scanned from $-20$ V to $+30$ V at a fixed drain bias. Subsequently, in order to clarify the effect of the gate bias, the irradiation step is carried out at fixed gate bias, and the experimental procedures are described in the following subsections. The transfer characteristics below were taken in linear regime on devices that had never been measured before, to ensure that there are no residual traps from prior operation. Similar results were obtained with another set of devices from the same substrate.

A. Irradiation without gate bias

In our first experiment, the OTFT was irradiated while the electrodes are kept floating. This procedure involves (1) exposing the transistor to green LED light for 1 min without gate bias and (2) measuring the electrical characteristics in dark. These steps are repeated to investigate the PPC effect under various light exposure times, as shown in Fig. 2. The channel width and length of this pure device are 674 µm and 63 µm, respectively. The source-drain voltage $V_{sd}$ is fixed at $+5$ V in these transfer characteristics measurements, and mobility extracted from the linear regime is 0.014 cm²/Vs. Since the transfer curves are not completely linear at the high gate bias, a limited range of drain current, with $V_g$ between 20 V and 30 V, is used to extracted mobility and threshold voltage by least square fitting (LSF). In Fig. 2(a), the sub-threshold region of the transfer curves are shifted by about 1 V in the negative direction as the cumulative light exposure increases. Another small change in the transfer characteristics is that, at gate bias beyond the threshold voltage $V_t$, the source-drain current has decreased with light exposure in Fig. 2(b). The threshold voltage shows negligible change.

B. Irradiation with gate bias

When a gate field is present, the photo-generated carriers may move toward the front and back channel. This carrier separation enhances PPC in certain condition as found below. The stress conditions involve varying bias polarity (positive or negative gate bias) and light exposure (light on or off). The source and drain electrodes are held at ground during gate bias stress. For these OTFTs, the stress condition that causes the most severe PPC is the combination of a negative gate bias with light exposure. With severe PPC, the effect lasts for some time and interferes with subsequent measurements. Thus, the sequence of applying these stress conditions is applied based on this consideration, combination of a negative gate bias with light exposure is tested last. The bias voltage of ±20 V is used because it is a typical

Measurements were done on OTFTs with a neat semiconductor or a blend semiconductor film.

FIG. 1. A top-gate transistor is irradiated by light from the top. Fixed amount of scattered light enters the semiconductor layer from the bottom and mobile charge carriers are generated.

FIG. 2. (a) When the cumulative light exposure increases, the sub-threshold current increases and the transfer characteristics shift slightly to the negative direction. (b) Same data in the linear scale.
operational voltage range. The experimental procedure is summarized in Table I.

Positive gate bias stress in the dark does not significantly change the device characteristics in the above measurements. However, with light exposure and negative gate bias, the subthreshold current increased by up to two orders of magnitude in Fig. 3(a), exhibiting a negative shift of about 10 V. The threshold voltage is also shifted in the negative direction as shown in Fig. 3(b). The $V_t$ shift observed in this case is close to 3 V, and this is much larger than that in Fig. 2(b) where a gate bias was not applied during irradiation. The device mobility did not show significant change throughout these measurements. The other three stress conditions did not lead to PPC.

C. Recovery in the dark

Following the stress measurements, the OTFTs are kept in dark, and the changes in transfer characteristics are monitored. As shown in Fig. 4(a), the persistent photoconductivity diminishes over a timescale of minutes to hours, and the device gradually returns to its original characteristics. Four days after the stress, the original characteristics is completely restored for this device with neat semiconductor. The recovery process is shown to accelerate at 60 °C compared to at room temperature.

D. Transistor with a blend semiconductor

The above procedures were repeated with the blend device. The channel width and length of this blend device are 681 μm and 59 μm, respectively. The mobility extracted from the linear regime is 0.010 cm²/Vs. Similar trends are found when comparing to the device with neat semiconductor, such that the irradiation effect without gate bias is minimal (Fig. 5), whereas significant shift is observed with irradiation under negative gate bias (Fig. 6). The blend OTFT exhibits a sharper subthreshold slope (2 V/decade)

<table>
<thead>
<tr>
<th>Step</th>
<th>Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Stress the OTFT with positive gate bias for 1 min.</td>
</tr>
<tr>
<td>2</td>
<td>Measure electrical characteristics in the dark.</td>
</tr>
<tr>
<td>3</td>
<td>Stress the OTFT with the positive gate bias and the LED light on for 1 min.</td>
</tr>
<tr>
<td>4</td>
<td>Measure electrical characteristics in the dark.</td>
</tr>
<tr>
<td>5</td>
<td>Repeat Steps 1–4 with negative gate bias</td>
</tr>
<tr>
<td>6</td>
<td>Keep the OTFT in the dark without gate bias; take periodic electrical measurements to monitor recovery</td>
</tr>
</tbody>
</table>

FIG. 3. (a) Transfer curves before and after the four stress conditions. The stress condition of irradiation (1 min) under the negative gate bias causes the most significant change in the transfer characteristics. The sub-threshold current increases and the threshold voltage shifts in the negative direction. (b) Same data in the linear scale.

FIG. 4. Comparison of the recovery process at (a) 25 °C and (b) 60 °C in a device with neat semiconductor.
than the neat device (4 V/decade). However, the recovery process in a blend device is slower than a neat device (Fig. 7). The recovery is not complete after four days in the dark at room temperature.

IV. DISCUSSIONS

The two light-induced effects, namely the negative shift in threshold voltage and the increase of the sub-threshold current, are influenced by the gate bias, and therefore mechanisms of the PPC effect are clarified by analyzing the bias dependence in the Secs. IV A and IV B. Moreover, the device response to light can be used as a diagnostic tool for OTFT development.

A. Threshold voltage shift

Threshold voltage shifts in the negative direction with light exposure. The magnitude of $V_t$ shift is much larger if a gate bias is present during irradiation. Comparing Figs. 2 and 3, net positive fixed space charges are generated by the illumination.
There are three possibilities for the location of the fixed charges, namely, in the bulk, at the dielectric/semiconductor channel interface ("front channel"), or at the semiconductor/substrate interface ("back channel"). When the gate field is not present during illumination, photo-generated carriers can only diffuse and most of them recombine. However, some holes are trapped in the bulk, while electrons are more mobile in the n-type material and they are likely to be swept away. This leads to the schematic in Fig. 8(a). When the gate is negatively biased during illumination, photo-generated carriers are separated, and holes accumulate at the dielectric/semiconductor channel. Some holes are trapped there and represent a distribution of positive fixed space charges as illustrated in Fig. 8(b). It is possible that some holes are trapped in the bulk before reaching the front channel during the drift under the external field. It is also possible to have negative charges fixed in the bulk or at the back channel, as long as the net fixed charge density is positive. As the recovery process is observed to be faster at an elevated temperature, the trapped holes are thermally released. This indicates that heating is a potential method to suppress PPC effects.

A previous report has shown that light exposure reverses the bias-stress effect in polymer transistors, because the charges trapped in the semiconductor are recombined with photo-generated charges. This explanation is applicable to our observations. Charged meta-stable states are correlated to the threshold voltage shift as follows. Let \( N_{\text{ns}} \) be the number of meta-stable states per unit area and add \( N_{\text{ms}} \) to the channel charge \( Q_{\text{ch}} \) in the gradual channel approximation.

\[
Q_{\text{ch}}(x) = C_i [V_g - V_f - V(x)] + qN_{\text{ms}}, \tag{1}
\]

where \( C_i \) is the capacitance of the gate insulator per unit area, \( x \) is the coordinate for the channel direction, \( V(x) \) is the surface potential, \( V_g \) and \( V_f \) are gate and threshold voltage, and \( q \) is the elementary charge. The integration of Eq. (1) gives the following equations for the drain current:

\[
I_d = \mu C_i \frac{W}{L} \left( \frac{V_g - V_f}{2} \right) V_d, \tag{2}
\]

\[
I_d = \mu C_i \frac{W}{L} \left( \frac{V_g - V_f + \Delta V}{2} \right)^2, \quad \text{for } V_d > V_{\text{dsat}}, \tag{3}
\]

where

\[
\Delta V = \frac{qN_{\text{ms}}}{C_i}, \tag{4}
\]

\[
V_{\text{dsat}} = V_g - V_f + \Delta V. \tag{5}
\]

The threshold voltage shift and the density of meta-stable states are related by Eq. (4). The threshold voltage shift observed in Fig. 2 is about 0.4 V and corresponds to \( 1 \times 10^{10} \text{ cm}^{-2} \) charged states while the \( V_f \) shift in Fig. 3(b) is 2.8 V implies that the \( N_{\text{ms}} \) density is \( 8 \times 10^{10} \text{ cm}^{-2} \). These are for the transistor printed with the neat semiconductor, and the blend device shows similar numbers.

The threshold voltage change in our blend OTFT is more persistent than the neat device. In the blend devices at room temperature, the recovery process was not complete after four days in the dark. The slower trap release rate in blend OTFTs might be due to impeded transport in the insulating polymer of the blend. Or, it is also possible that irreversible chemical change has occurred, as photo-induced oxygen doping has been reported in a polymer semiconductor, and oxygen exposure under a positive gate bias increased sub-threshold current in a pentacene transistor. The rate of stress and recovery follows the phenomenological stretched exponential expression common in disordered semiconductor, but since the stretched exponential is only a phenomenological model, further experiments are underway to identify the shallow and deep trap states in these devices.

**B. Sub-threshold current**

The increase of sub-threshold current is significant in the stress condition with light and negative gate bias. The subthreshold models developed for OTFTs treat the off-state as a junction-type field-effect transistor. The sub-threshold region corresponds to charge accumulation in the localized states, typically band tail states, as the gate voltage is increased. Before the irradiation and negative gate bias stress, there is little fixed charge at the interface, and the OTFT is depleted. Whereas after irradiation with negative gate bias, there is positive meta-stable charge, which induce a conduction channel. It takes a larger negative gate voltage to deplete the channel as illustrated in Fig. 9.

If the positive charge in the above discussion is a sheet-like distribution of fixed charge at the dielectric interface, then the transfer characteristics would simply be translated in the negative direction. However, that is not the case in Figs. 3(a) and 6(a), where the sub-threshold region is shifted much more than \( V_f \) with the light exposure. To explain the...
diagnostic tool for transistor process development, and modifying the back-channel interface to minimize PPC will be investigated in the future.

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